

Application No. 10/735996 (Docket: CNTR.2152)
37 CFR 1.111 Amendment dated 05/22/2007
Reply to Office Action of 02/22/2007

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REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are pending in the application. The Examiner additionally stated that claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are rejected. By this amendment, claims 1, 11, and 21 are amended. Hence, claims 1, 3-5, 8-11, 13-15, 17-25, and 27-29 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Claims

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 1, 11, and 21 under 35 U.S.C. 103(a) as being unpatentable over the background of the specification in view of Philip, U.S. Patent No. 3,130,387 (hereinafter, "Philip"). Applicant respectfully traverses the Examiner's rejections.

The Examiner noted that the background of the instant application specification teaches a microprocessor apparatus, for precluding a pipeline stall due to microcode ROM access delay, the microprocessor apparatus comprising:

- a translator, configured to generate a plurality of micro instructions corresponding to an instruction and a microcode entry point (Spec: 0007);
- early access logic, couple to said translator, configured to employ said microcode entry point to access a microcode ROM prior to when said microcode entry point is provided to register logic, whereby said microcode ROM provides a first micro instruction to said register logic when said first micro instruction is required by said register logic, and wherein said translator provides said plurality of micro instructions to said register logic (Spec: 0009) (The Examiner stated that all of this inherently flows from the specification and that it would be inefficient to have another unit generate the ROM address when the translator is already determining what the instruction is.); and